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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,936	12/21/2001	Christopher M. Giles	L13.12-0180/01-297	2648
7590	06/30/2004		EXAMINER	
Sandeep Jaggi, Ph. D. LSI LOGIC CORPORATION M/S D-106 1551 McCarthy Boulevard Milpitas, CA 95035			THAI, XUAN MARIAN	
			ART UNIT	PAPER NUMBER
			2111	
DATE MAILED: 06/30/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/027,936	GILES, CHRISTOPHER M.	
	<b>Examiner</b>	<b>Art Unit</b>	
	XUAN M. THAI	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 21 December 2001.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6, 8-9, 11-14, 16 and 17 is/are rejected.  
 7) Claim(s) 7, 10 and 15 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 21 December 2001 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

**DETAILED ACTION**

1. This is in response to communication filed on December 21, 2001. Claims 1-17 are pending in the application.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Balakrishnan (USPN 5,122,691).

As per claims 1, 13 and 17, Balakrishnan teaches a platform comprising: a backplane (Fig. 5) providing a plurality of busses; a plurality of system bus cards (90-107), each of the system bus cards comprising: a system bus (e.g. 83; fig. 6; col. 9, lines 49 et seq.; 171; fig. 7; col. 10, lines 3-10); a bus infrastructure device (e.g. bus chip(s); col. 9, lines 2-15); a plurality of daughter cards (modules 110-117; col. 9, lines 1-35).

As per claim 2, Balakrishnan teaches a multi-master/multi-slave card couple to the backplane and at least one interface to busses on the backplane (e.g. control module; col. 17, lines 25 et seq.)

As per claim 3, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises a bus arbiter (col. 17, lines 25-31).

As per claim 4, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises an address decoder (col. 17, lines 19-30).

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As per claims 5 and 6, wherein the system bus of each of the plurality of system bus cards further comprises a multi-master bus and a multi-slave bus, and wherein when daughter cards are physically coupled to a particular system bus card, master and slave devices on the daughter cards are electrically coupled to the multi-master bus and the multi-slave bus, respectively (col. 9, lines 1-35; col. 17, lines 1-30).

As per claim 14, wherein for each of the plurality of system bus cards, the corresponding daughter cards coupled to that system bus card function with the system bus card to model a corresponding system bus on an integrated circuit to be implemented (modules 110-117; col. 9, lines 1-35; col. 10, line 60 – col. 11, line 2).

As per claim 16, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises a bus arbiter and an address decoder (col. 17, lines 19-30).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan (USPN 5,122,691) in view of Chang (USPN 6,526,525).

As per claim 8, Balakrishnan teaches the claimed invention as stated above except for a bus card comprises a debugging device which aids in debugging errors in the system. Chang teaches a bus card comprises a debugging device (fig. 4; abstract).

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At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the Balakrishnan system to incorporate the debugging device on the bus card as taught by Chang to arrive at the claimed invention. Chang suggests that for the engineers engaged in PC hardware maintenance and development as well as researchers and students experimenting with PC, debugging bus card is an indispensable tool (e.g. col. 2, lines 39 et seq.).

6. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan (USPN 5,122,691) in view of Davies et al. (US 2002/0019924 A1; Davies).

As per claim 11, Balakrishnan teaches the claimed invention as detailed above except for daughter card comprising a CPU or IP device. Davies, in his a reconfigurable processing system architecture allows for a CPU or IP device to be implemented on a daughter card (see Abstract and para [0018]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a daughter card containing a CPU in the system of Balakrishnan, as taught in the system of Davies, in that Davies stated that the implementation would allow for a variety of processing system configurations to be implemented in a single device; such implementation would allow for flexibility in system configuration (Abstract); therefore being advantageous.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan (USPN 5,122,691)

As per claim 12, Balakrishnan teaches the claimed invention as detailed above except for the daughter card comprising a graphics engine device. The examiner takes Official Notice that

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at the time the invention was made, daughter cards comprising a graphics engine device is common practice as exemplified in Publication No. RD 408012A.

*Allowable Subject Matter*

8. Claims 7, 10 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per claims 7 and 10, Applicant claims a configurable and scaleable multi-bus platform, wherein each system bus card further comprises a statistic generating device coupled to the system bus' the statistic generating device generating statistical information indicative of the performance of the system. Prior art of record do not teach these features.

As per claim 15, Applicant claims a platform further comprises a multi-master/multi-slave multi-bus-port card which is physically coupleable to the backplane, wherein the multi-master/multi-slave multi-bus-port card includes at least one interface device, and wherein when the multi-master/multi-slave multi-bus-port card is physically coupled to the backplane then at least one interface device in electrical communication with one or more of the busses provided by the backplane. Prior art of record do not teach the combination of these features.

*Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached Form PTO-892.

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10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



XUAN M. THAI  
Primary Examiner  
Art Unit 2111

XMT